Pi 2 Media

PI2AES
Digital Pro Audio Hat
Hardware Reference Manual

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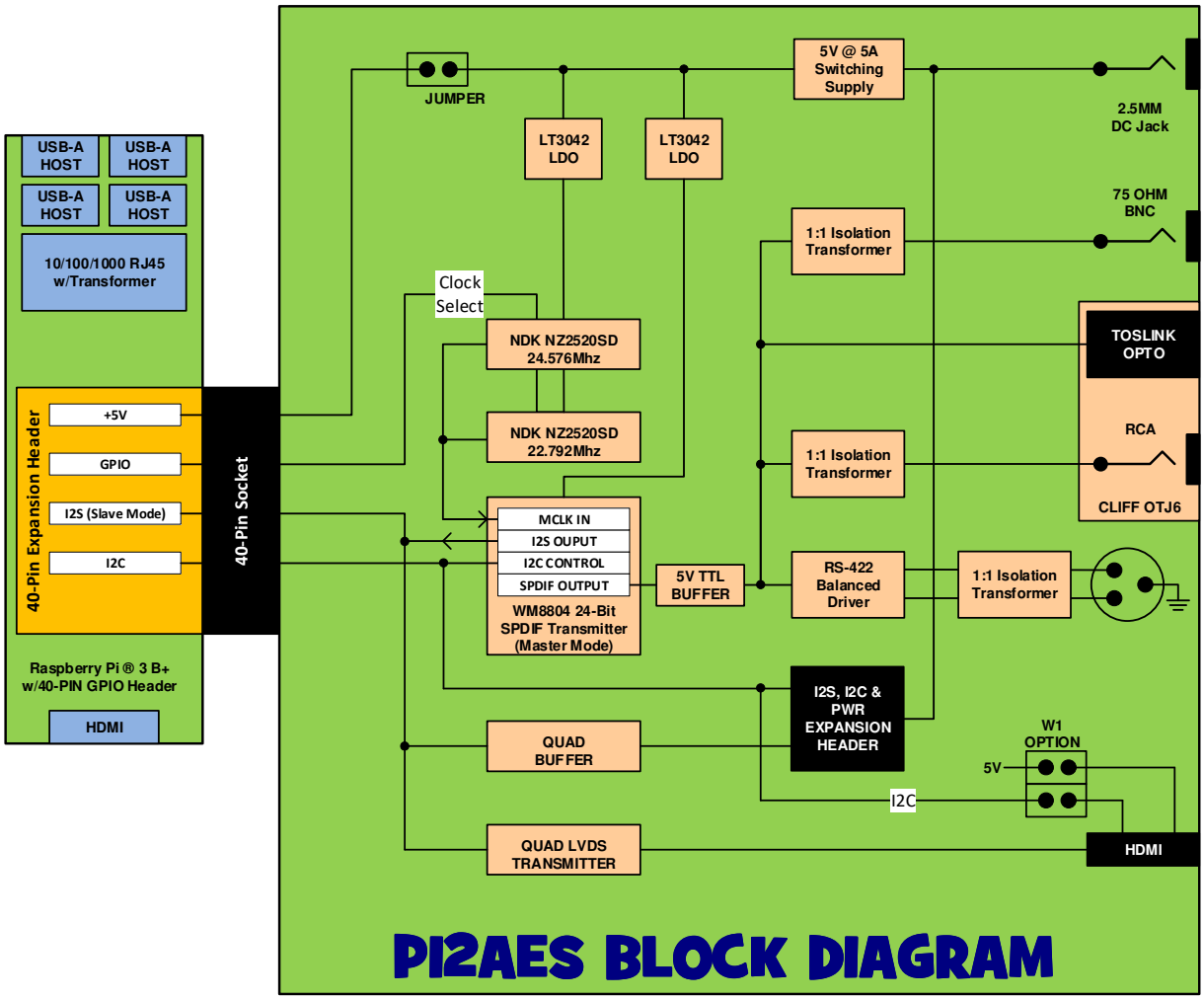

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2 OPERATING SPECIFICATIONS

2.1 PI2AES OPERATING SPECIFICATIONS

The PI2AES conforms to the following specifications:

Specification	Value
Dimensions	85mm x 56.5mm
Weight	~10g
Storage Temperature	-20C to +85C
Operating Temperature	0C to +70C
Humidity	0% to 95% RH, Non-Condensing
Input Voltage (VIN)	+24V to +48V
Power Consumption	250mw Typical, 1W Maximum

Table 1 – PI2AES Operating Specifications

3 OVERVIEW

3.1 INTRODUCTION

The PI2AES, designed and manufactured by PI 2 Design, is a professional I/O Shield designed to bring Professional Studio Grade Audio to the Raspberry PI ® family of Single Board Computers. This low-cost Shield converts the Raspberry Pi ® I2S Interface to High Definition Digital Audio Coax, OPTO and Balanced XLR.

The addition of Parallel I2S Output along with LVDS Differential over HDMI allows the PI2AES to interface with virtually any High Performance DAC on the market.

The major features of the PI2AES are as follows:

- **FORM FACTOR –** Raspberry Pi ® Shield Size w/40-Pin mating connector.
- **AES TRANSMITTER –** The industry standard WM8804 converts the RPi I2S stream to AES3/SPDIF formatted data at 24-Bit up to 192Khz Frame Rate
- **SPDIF COAX OUTPUT –** An RCA connector with Isolation Transformer provides coaxial transmission of the SPDIF Audio Data Stream.
- **SPDIF OPTICAL OUTPUT –** Isolated Optical Transmitter Supports Consumer Level DAC and AVR inputs
- **AES BNC OUTPUT -** A 75 ohm BNC connector with Isolation Transformer provides for Single Ended AES transmission.
- **AES BALANCED OUTPUT –** An RS-422 Transmitter coupled with Isolation Transformer allows the transmission of balanced audio data with 110 ohm impedance via the Professional Audio Standard XLR Connector
- **BUFFERED I2S OUTPUT –** Parallel Buffered I2S is available for direct short distance connection to off-board D/A. Perfect for DIY use! I2C for control is also provided as well as 5V Regulated and Input Voltage Rails.
- **DIFFERENTIAL I2S OUTPUT –** A DS2063 Differential Transmitters is used to drive the I2S Bus over a standard HDMI Connector. The Pinout is Selectable Between the PS Audio and Gustard Standards.
- **HIGH RESOLUTION CLOCKS –** A pair of Ultra-Low Noise NDK NZ2520SD oscillators allow the WM8804 to operate in non-PLL mode for the lowest possible noise.
- **ULTRA-LOW NOISE LDO's –** Ultra-Low Noise AP1155ADL LDO (30uV noise and 80dB PSRR) is used to Supply the WM8804 Transmit Section, while an ADP150 (9uV noise and 70dB PSRR) and the High-Resolution Clocks.
- **LOW NOISE PCB LAYOUT** – Constructed with 4-layer Split Ground PCB with noise reduction techniques refined from years of High-Speed Mixed-Signal Design work

3.2 BLOCK DIAGRAM

Refer to the following figure for a block diagram of the PI2AES Shield.

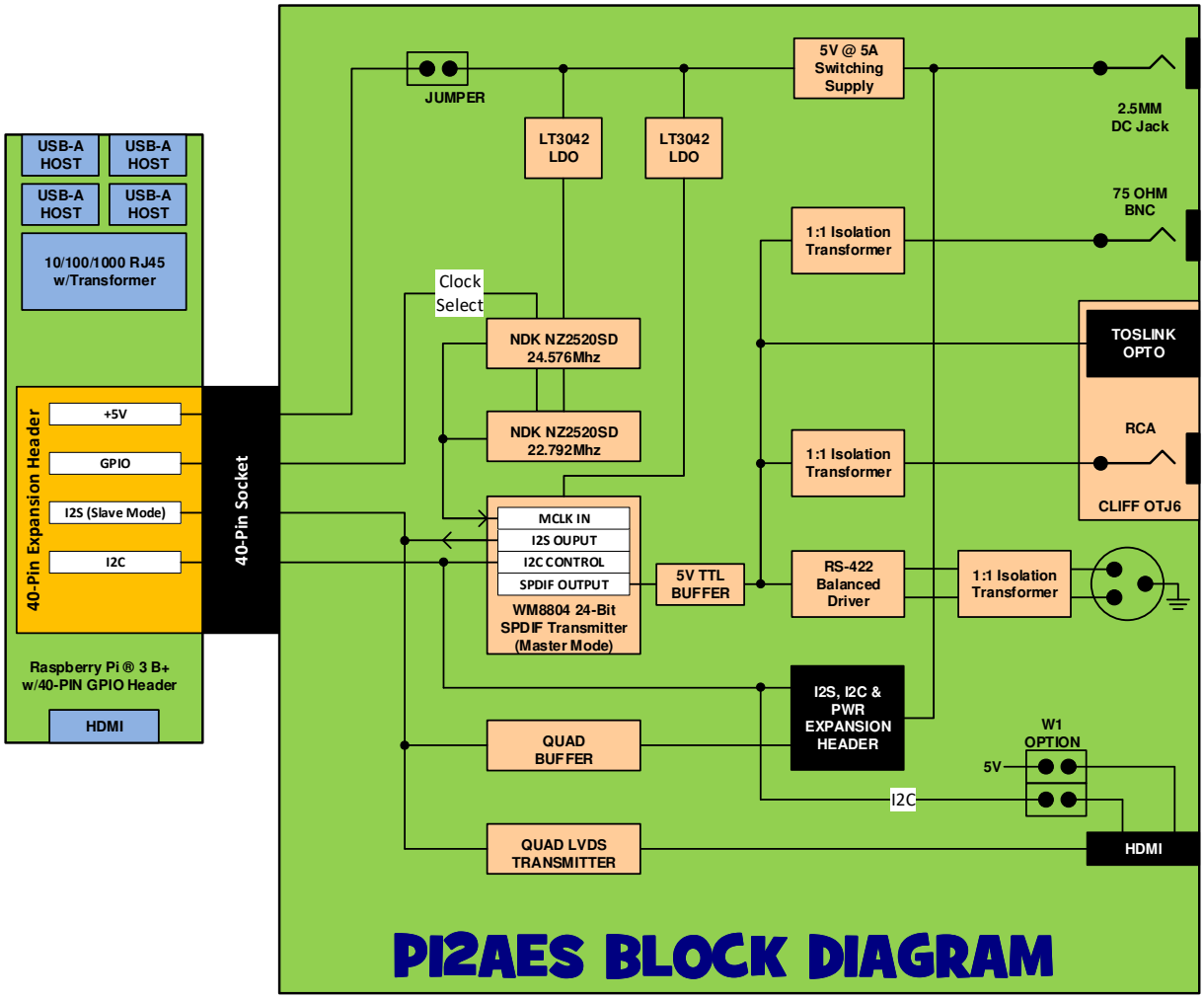


Figure 1 – PI2AES Block Diagram

4 ON-BOARD DEVICES

4.1 *OVERVIEW*

The PI2AES interfaces to the RPi via the 40-Pin GPIO Connector. This section describes in detail the devices located on the PI2AES.

4.1 PI2AES I2C BUS DEVICES

The following table describes the CPU I2C Bus usage of the PI2AES. Most of these addresses are set by the startup script supplied by Pi2Design. Refer to the respective device documentation for more detail.

I2C Bus	7-Bit I2C Address	Description
I2C	0x3B	WM8804 SPDIF Transmitter

Table 2 – PI2AES I2C Bus Devices

4.1 WM8804 SPDIF TRANSMITTER

At the core of the PI2AES is the Cirrus Logic WM8804 AES Digital Audio Transmitter. This device interfaces to the Raspberry Pi via I2S and I2C. The signals used to interface with the WM8804 are shown in the following table.

WM8804 Signal	RPi Signal	Description
MCLK	-	Unused
BCLK	BCLK	I2S Bit Clock Output to Pi
LRCLK	LRCLK	I2S Word Clock Output to Pi
SDIN	SDOUT	I2S Serial Audio Data Input from Pi
SCL	SCL	I2C Clock from Pi
SDA	SDA	I2C Data to/from Pi
XIN	GPIO5	1 = Select 22.5792Mhz Input Clock for 44.1Khz, 88.2Khz and 176.4Khz Frame Rates
XIN	GPIO6	1 = Select 24.576Mhz Input Clock for 48Khz, 96Khz and 192Khz Frame Rates

TXO	-	AES3/SPDIF encoded digital audio output

Table 3 – RPi to WM8804 Connections

4.1.1 WM8804 SPDIF TRANSMITTER NOTES

1. The WM8804 is controlled using the I2C port. Refer to the WM8804 documentation and Pi 2 Design supplied driver code for more detail.
2. The PI2AES is designed to operate the WM8804 in Master mode. In this mode the WM8804 receives its master clock from XIN and drives MCLK (unused), BCLK and LRCLK to the Pi. Serial Data in is received from Pi.
3. Pi GPIO's 6 and 13 are used to select the desired clock input. GPIO 6 and 13 are pulled low by default. CAUTION - Do not select more than one clock at a time!

4.2 DUAL HIGH RESOLUTION NDK CLOCKS

A pair of NDK NZ2520SD Ultra-Low Noise clocks provide the critical timing signals for the WM8804. They are selected via Raspberry PI GPIO5 (22.5792Mhz) and GPIO6 (24.576Mhz).

4.3 RS-422 DIFFERENTIAL TRANSMITTER

An RS-422 Differential Transmitter accepts the SPDIF output from the WM8804 and sends it as a balanced pair to the 1:1 Isolation Transformer and then to the XLR connector.

4.4 I2S PARALLEL BUFFER

A 74FCT125 CMOS Buffer is used to drive the I2S signals (MCLK, BCKL, LRCLK and SDO) to the I2S Expansion Header. This device is designed to drive the I2S Bus short distances (<12 inches).

4.5 I2S DIFFERENTIAL DRIVER

A DS2063 Quad Differential LVDS Driver takes the I2S Bus and converts each signal into a balanced differential signal. This is then connected to the HDMI connector. This device is designed to drive the I2S Bus up to 3 meters.

4.6 AUDIO DATA RATE AND POWER LED'S

A triple stack LED is used to provide visual indication of: Power On (Green), Audio Data Rate of 48/96/192Khz (Yellow) and Audio Data Rate of 44.1/88.2/176.4Khz (Red).

5 RPI GPIO

5.1 OVERVIEW

The PI2AES uses a number of signals from the RPi GPIO header for control and status purposes. This usage is defined in the following table.

RPi PIN	DIR	AF	PUP/ PDN	PI2AES Name	Description/Notes
1	-	-	-	-	RPi +3.3V - Unused
2	-	-	-	+5V	+5V Power to/from the RPi
3	I/O	Y	PUP	I2C_SDA	I2C Bus Data
4	-	-	-	+5V	+5V Power to/from the RPi
5	OUT	Y	PUP	I2C_SCL	I2C Bus Clock
6	-	-	-	GND	
7	OUT	-	-	GPIO4	Unused
8	-	-	-	GPIO14	Unused
9	-	-	-	GND	Unused
10	-	-	-	GPIO15	Unused
11	-	-	-	GPIO17	Unused
12	IN	Y	-	BCLK	I2S Bit Clock from WM8804
13	-	-	-	GPIO27	Unused
14	-	-	-	GND	
15	-	-	-	GPIO22	Unused
16	-	-	-	GPIO23	Unused
17	-	-	-	-	RPi +3.3V - Unused
18	-	-	-	GPIO24	Unused
19	-	-	-	GPIO10	Unused
20	-	-	-	GND	
21	-	-	-	GPIO9	Unused
22	-	-	-	GPIO25	Unused

RPi PIN	DIR	AF	PUP/ PDN	PI2AES Name	Description/Notes
23	-	-	-	GPIO11	Unused
24	-	-	-	GPIO8	Unused
25	-	-	-	GND	
26	-	-	-	GPIO1	Unused
27	I/O	Y	-	ID_SDA	Unused
28	OUT	Y	-	ID_SCL	Unused
29	-	-	-	GPIO5	1 = Select 22.5792Mhz Clock Input to WM8804
30	-	-	-	GND	
31	OUT	-	PUP	GPIO6	1 = Select 24.576Mhz Clock Input to WM8804
32	-	-	-	GPIO12	Unused
33	OUT	-	-	GPIO13	Unused
34	-	-	-	GND	
35	IN	Y	-	LRCLK	I2S Left/Right Clock from WM8804
36	-	-	-	GPIO16	Unused
37	-	-	-	GPIO26	Unused
38	-	-	-	GPIO20	Unused
39	-	-	-	GND	
40	OUT	Y	-	SDOUT	Pi I2S Serial Audio Data Out

Table 4 – CPU GPIO Pin Assignments

5.1.1 RPI GPIO NOTES

1. DIR is from the point of view of the RPi.
2. Y in the Alternate Function (AF) column indicates that the use of this pin requires the pin to be assigned to the function as defined by the RPi specifications.
3. PUP/PDN indicates if the GPIO should have its associated Pullup (PUP) or Pulldown (PDN) resistor enabled.
4. An asterisk '*' at the beginning of the name indicates a low true signal.

6 PI2AES POWER

6.1 OVERVIEW

The PI2AES is designed to be powered from an external +24V to +48V source. Jumper W2, when installed, allows the Raspberry PI to be powered from the PI2AES. When jumper W2 is removed, separate 5V power must be supplied to the Raspberry PI.

Note that an on-board protection circuit ensures proper operation when jumper W2 is installed while power is applied via J1 AND from the Pi (P1) simultaneously.

See the below block diagram for a simplified view of the PI2AES power.

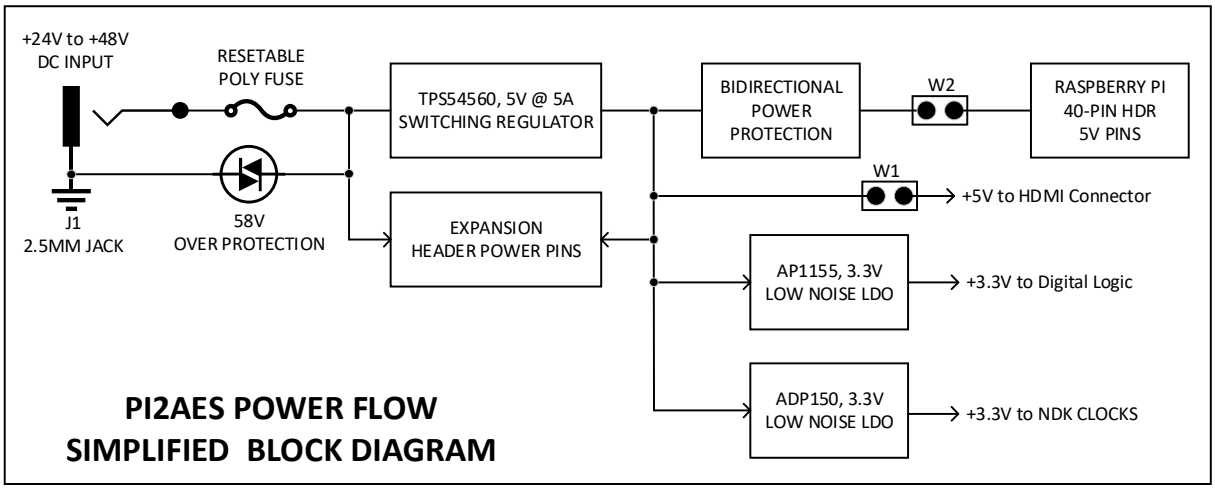


Figure 2 – PI2AES Power, Simplified Block Diagram

7 PI2AES SOFTWARE

7.1 OVERVIEW

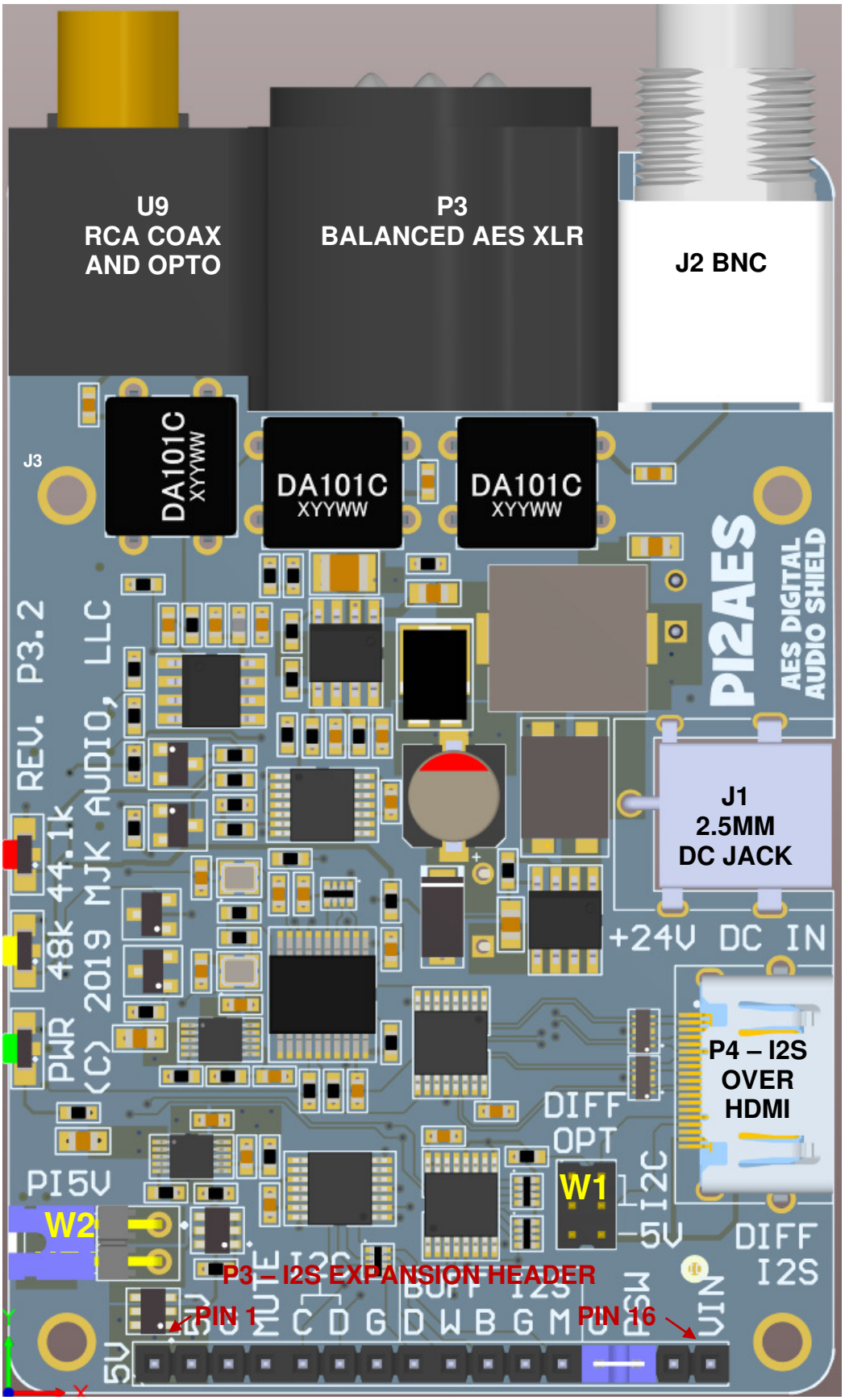
Due to the various resources interfaced on the PI2AES, both internal and external to the RPi, it is necessary to initialize a large number of CPU registers and external devices before correct operation can begin. These values and their proper sequencing are beyond the scope of this document. See our web site at http://www.pi2design.com or email us at support@pi2design.com for example operating and initialization code.

Note that for standard Audio Player software, the PI2AES can use the HifiBerry Digi+ Pro driver.

8 PI2AES CONNECTORS

8.1 OVERVIEW

This section provides the type, location and pinout for the various connectors on the PI2AES. Top View is shown in the following 3D render.


U9
RCA COAX
AND OPTO
P3
BALANCED AES XLR
J2 BNC
J3
DA101C
XYYWW
DA101C
XYYWW
DA101C
XYYWW
PI2AES
AES DIGITAL
AUDIO SHIELD
REV. P3.2
(C) 2019 MJK AUDIO, LLC
PWR 48k 44.1k
J1
2.5MM
DC JACK
+24V DC IN
P4 – I2S
OVER
HDMI
DIFF
OPT
W1
I2C
PI5V
W2
5V
DIFF
I2S
P3 – I2S EXPANSION HEADER
PIN 1
PIN 16
5V
VIN

8.2 J1 – DC JACK

This jack is designed to accept a 5.5mm x 2.5mm center positive plug for external power in. Voltage must be +24V to +48V.

8.3 J2 – BNC

This 75 Ohm Jack is used to transmit Single Ended AES digital audio output.

8.4 P1 – 40-PIN GPIO HEADER (BOTTOM SIDE)

This is a standard 40-Pin .1" Dual Row Female Header. It is designed to accept a Raspberry Pi single board and conforms to the standard Raspberry Pi 40-Pin GPIO Header pinout.

8.5 P2 - I2S EXPANSION HEADER

This is a 16-Pin, .1" Single Row Header that carries I2S, I2C, and Power for expansion use. The Pinout for P2 is shown in the following table.

P2 PIN	Name	Description
1	5V	+5V direct from Regulator
2	5V	+5V direct from Regulator
3	GND	Ground
4	MUTE	1 = Mute On
5	SCL	I2C Clock
6	SDA	I2C Data
7	GND	Ground
8	SDO	Buffered I2S Data
9	LRCLK	Buffered I2S Left/Right (Word) Clock
10	BCLK	Buffered I2S Bit Clock
11	GND	Ground
12	MCLK	Buffered I2S Master Clock
13	GND	Ground
14	*PSW	Power Enable – Jumper with Pin 13 for auto on
15	NC	No Pin

16	VIN	+24V to +48V Input from DC Jack

Table 5 – I2S Expansion Header Pinout

8.1 P3 – XLR BALANCED OUTPUT

P3 is a 3-Pin XLR Connector. This 110-ohm connector carries the AES balanced digital audio output.

8.2 P4 – I2S OVER HDMI

P4 is a standard HDMI Connector that carries the Differential I2S signal. Pinout conforms to either the PS Audio (default) or Gustard standards. The Pinout for P4 is shown in the following table.

P4 PIN	Name	Description PS Audio Pinout	Description Gustard Pinout
1	SDO+	I2S Data Plus	I2S Data Plus
2	GND	Ground	Ground
3	SDO-	I2S Data Minus	I2S Data Minus
4	BCK+	I2S Bit Clock Plus	I2S Bit Clock Minus
5	GND	Ground	Ground
6	BCK-	I2S Bit Clock Minus	I2S Bit Clock Plus
7	LRCLK+	I2S Left/Right Clock Plus	I2S Left/Right Clock Minus
8	GND	Ground	Ground
9	LRCLK-	I2S Left/Right Clock Minus	I2S Left/Right Clock Plus
10	MCLK+	I2S Master Clock Plus	I2S Master Clock Plus
11	GND	Ground	Ground
12	MCLK-	I2S Master Clock Minus	I2S Master Clock Minus
13	NC	No Connect	No Connect
14	NC	No Connect	No Connect
15	SDA	I2C Data from W1 3-4	I2C Data from W1 3-4
16	SCL	I2C Clock from W1 5-6	I2C Clock
17	GND	Ground	Ground
18	+5V	+5V from W1 1-2	+5V from W1 1-2

P4 PIN	Name	Description PS Audio Pinout	Description Gustard Pinout
19	NC	No Connect	No Connect

Table 6 – I2S Over HDMI Pinout

8.3 W1 – I2S OVER HDMI OPTIONS

W1 is a 6-pin 2mm pitch header. It is used to enable the I2C and 5V options for the I2S over HDMI interface as follows.

W1 PINS	Name	Description, Jumper In
1-2	5V	Enable +5V to Pin 18 of the HDMI Connector P4
3-4	I2C_SDA	Enable I2C Data to Pin 15 of the HDMI Connector P4
5-6	I2C_SCL	Enable I2C Clock to Pin 15 of the HDMI Connector P4

8.4 U9 – COMBO RCA/OPTO TRANSMITTER

U9 is a Cliff OTJ6 that contains the RCA for SPDIF COAX digital audio output and a Toslink Transmitter for SPDIF Optical digital audio output.

9 DOCUMENT REVISIONS

Date	Revision	Change
03/26/2019	P0.1	Preliminary Release
06/02/2019	P2.0	Design Revision P2 Initial Release
08/15/2019	P3.0	Design Revision P3 Initial Release Added description of I2S over HDMI option block W1
08/16/2019	P3.1	Added entry for HifiBerry Digi+ Pro compatibility
11/23/2019	P3.2	Changed VIN range, now +24V to +48V
12/19/2019	P3.3	Corrected voltage range in Table 1

Table 7 – Document Revisions

IO ERRATA

10.1 OVERVIEW

Below is the current known errata for the PI2AES Rev. P3.x:

1. This revision changes no circuitry, but clarifies the required voltage range. It is now +24V to +48V.